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PATENT NUMBER and  
ISSUE DATE

U.S. UTILITY Patent Application

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10072533	02/08/2002	333		2817	
<b>**APPLICANTS:</b> Ishikawa Yohei; Sakamoto Koichi; Yamashita Sadao; Iio Kenichi;					
<b>**CONTINUING DATA VERIFIED:</b> THIS APPLICATION IS A DIV OF 09/031,981 02/26/1998 745255					
<b>** FOREIGN APPLICATIONS VERIFIED:</b> JAPAN 9-44162 02/27/1997					
PG-PUB DO NOT PUBLISH <input type="checkbox"/>		RESCIND <input type="checkbox"/>			
Foreign priority claimed 35 USC 119 conditions met <input checked="" type="checkbox"/> yes <input type="checkbox"/> no		ATTORNEY DOCKET NO			
Verified and Acknowledged Examiners's initials <i>Ray Lee</i>		P/1071-1520			
TITLE : Planar dielectric integrated circuit					

U.S. DEPT. OF COMM. / PAT. & TM. PTO-436L (Rev. 12-94)

<b>NOTICE OF ALLOWANCE MAILED</b>		<b>CLAIMS ALLOWED</b>	
		Assistant Examiner	Total Claims
			Print Claim for O.G.
<b>ISSUE FEE</b>		Primary Examiner	<b>DRAWING</b>
Amount Due	Date Paid		Sheets Drwg. Figs. Drwg. Print Fig. 7
<input type="checkbox"/> <b>TERMINAL DISCLAIMER</b>		<b>PREPARED FOR ISSUE</b>	Application Examiner
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